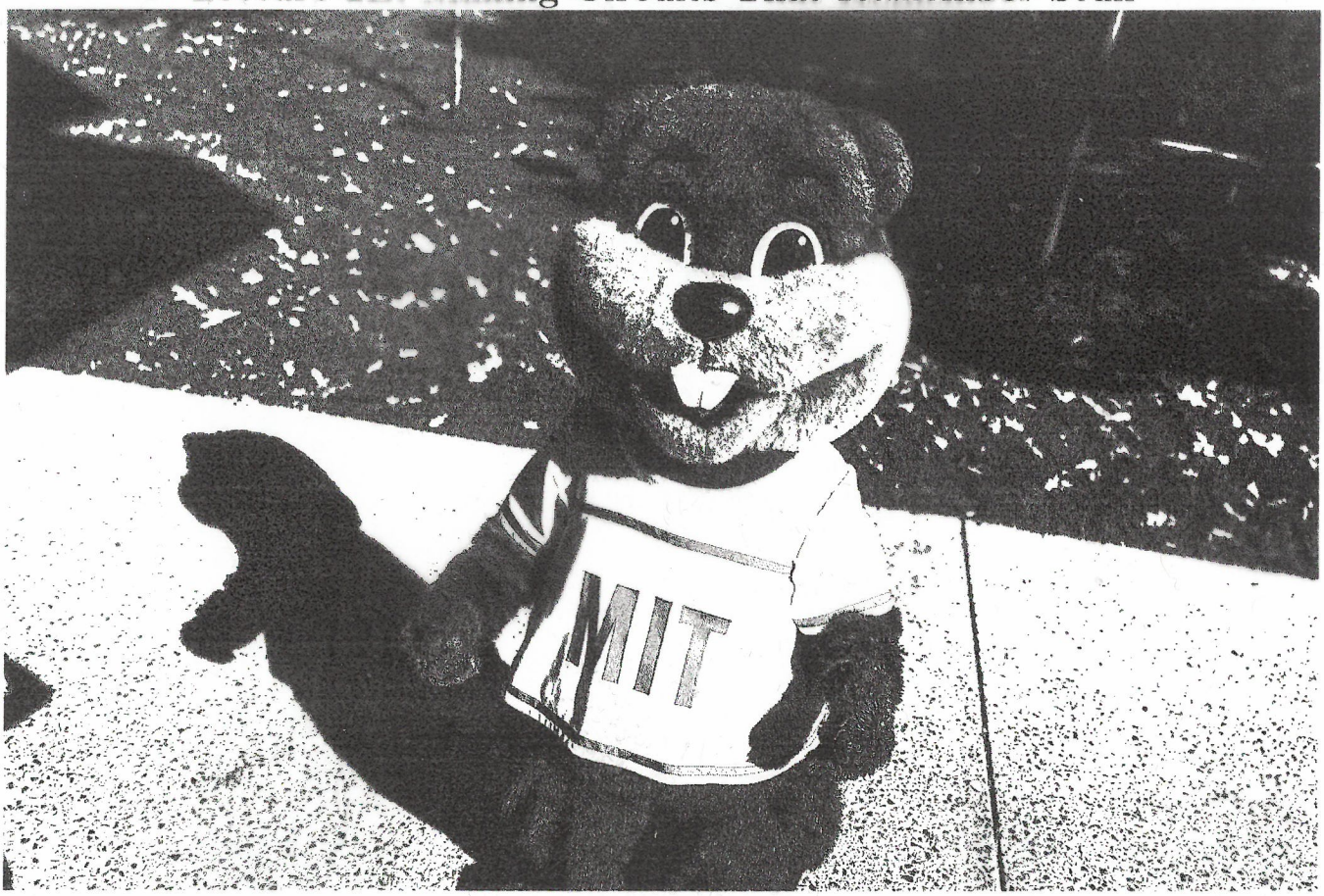
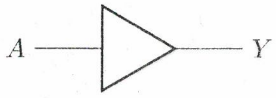
Build a Digital Clock from the 1980's

Lecture 2B: Making Circuits That Remember Stuff



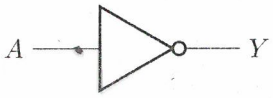
Original photo from `https://alum.mit.edu/slice/tim-beaver-exclusive-interview`
Edited using the GNU Image Manipulation Program (`https://www.gimp.org/`)

YES Gate



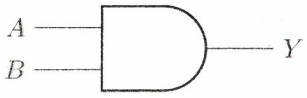
A	Y
0	0
1	1

NOT Gate



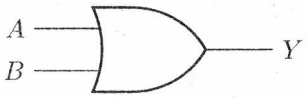
A	Y
0	1
1	0

AND Gate



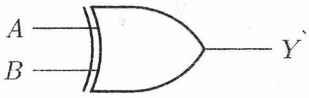
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate



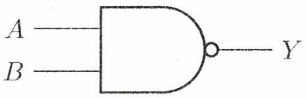
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

XOR Gate



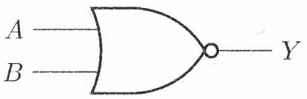
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

NAND Gate



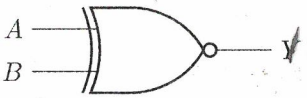
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate

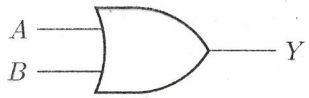


A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

XNOR Gate



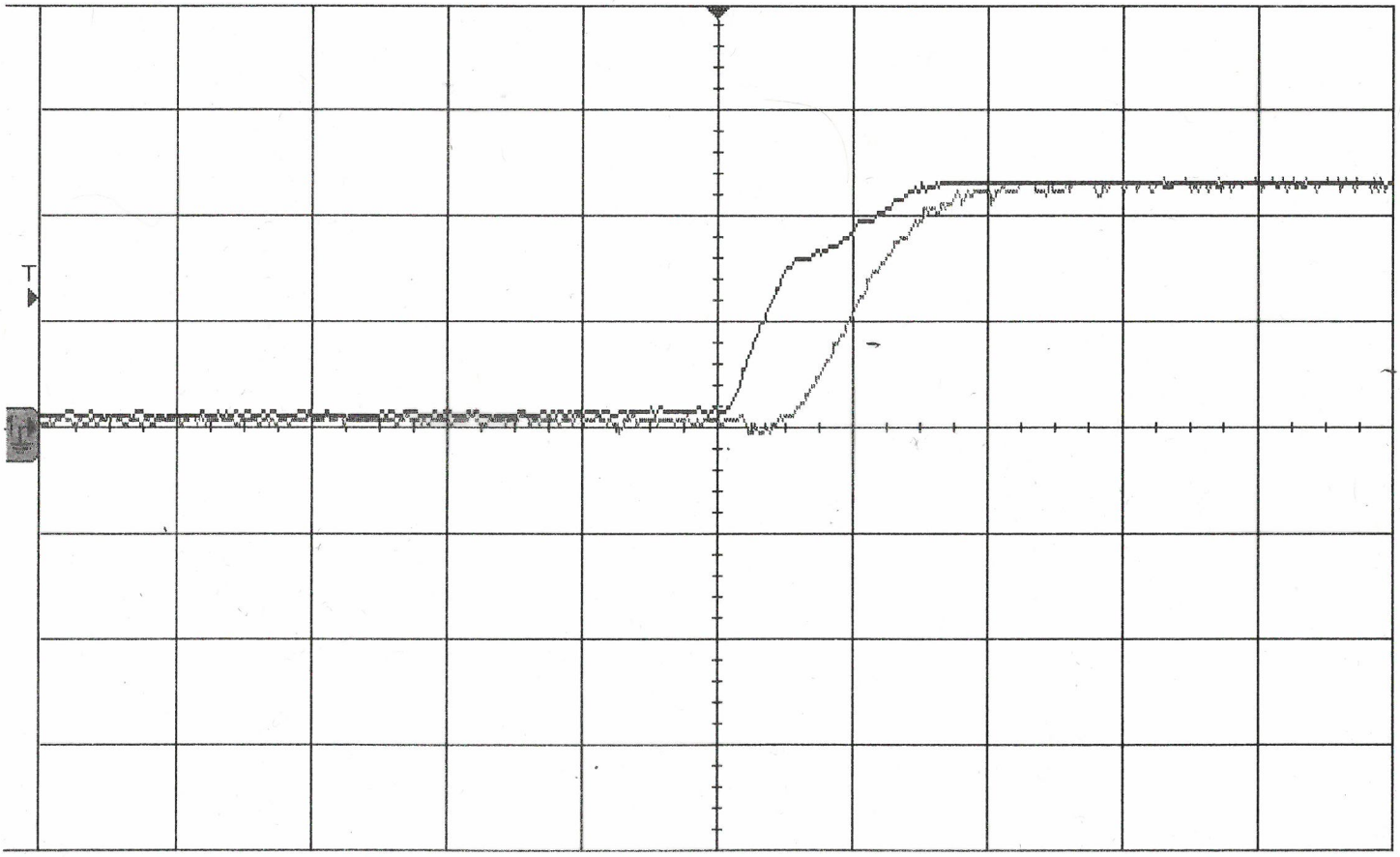
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

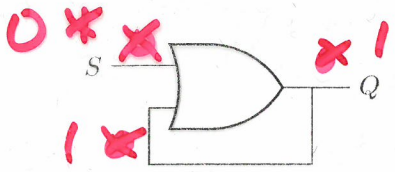


switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

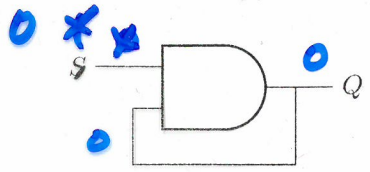
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 2 kΩ, C_L = 15 pF		14	22	ns
t_{PHL}					14	22	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

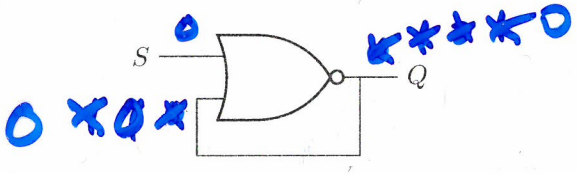




have i ever seen a 1?

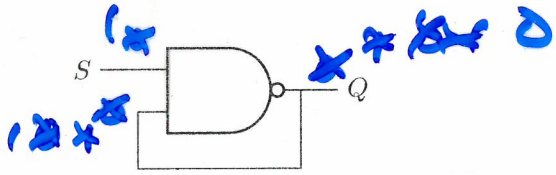


always zero



S = 0 → oscillate

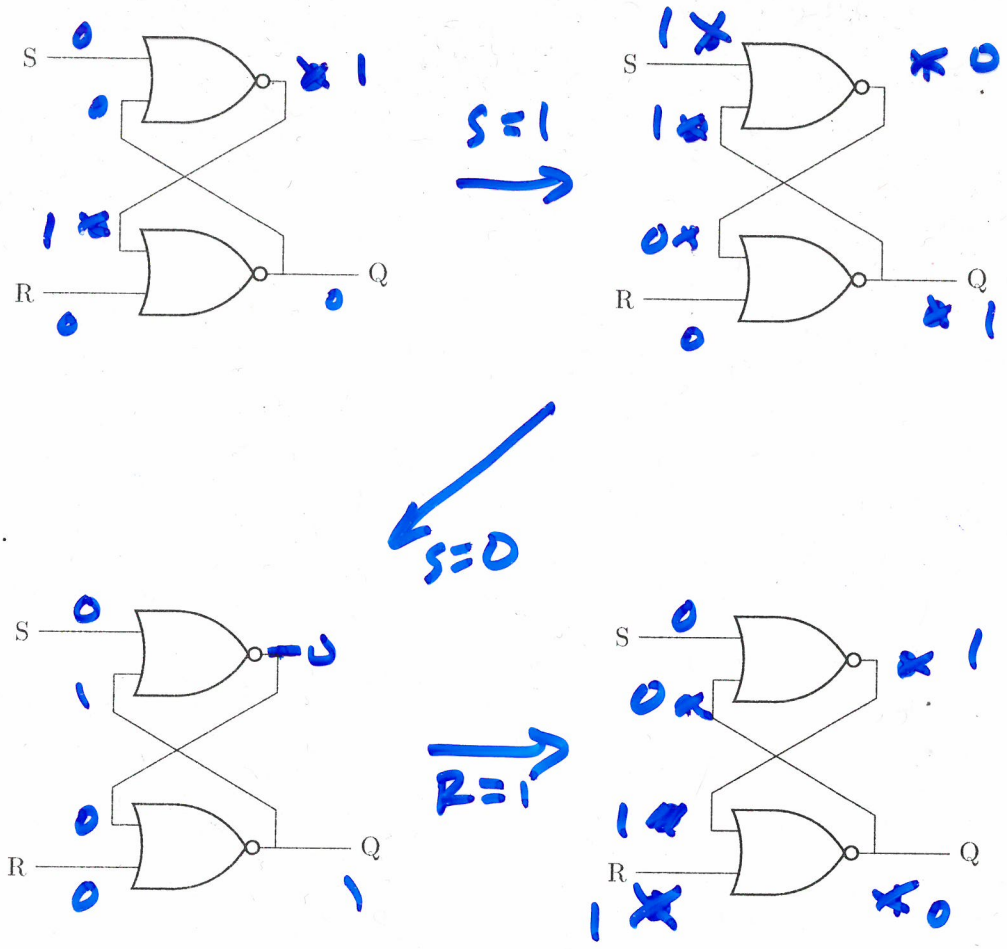
S = 1 → Q = 0



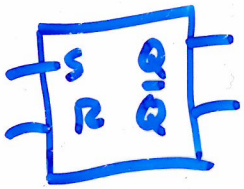
S = 0 → Q = 1

S = 1 → oscillation

ring oscillator

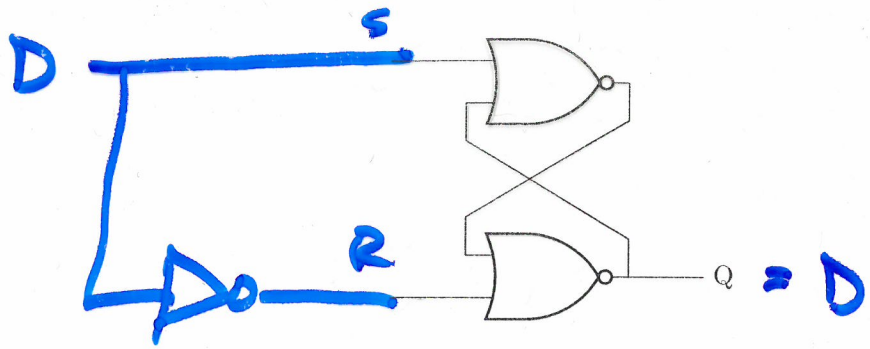


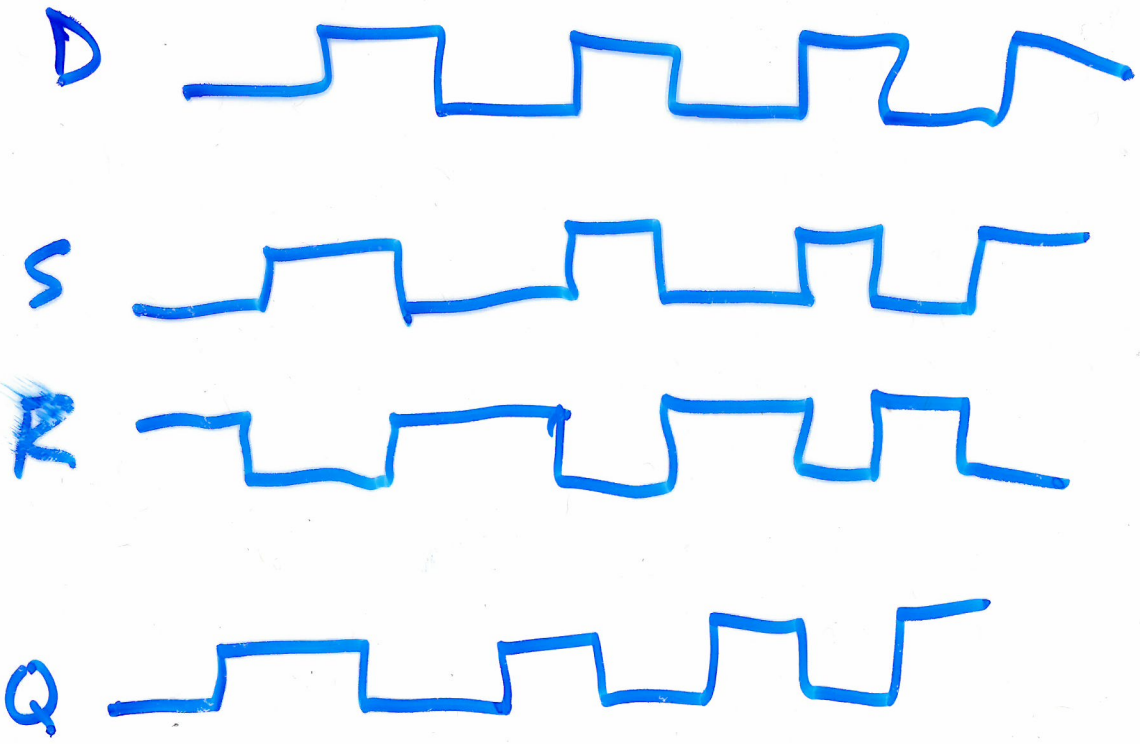
SR Latch

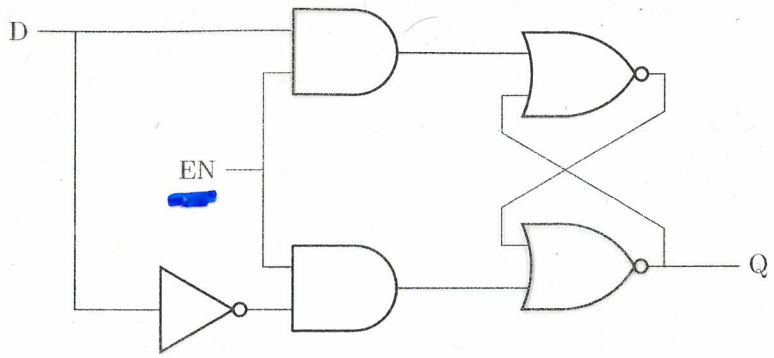


S	R	Q	$\bar{Q}$	
0	0	Same		
0	1	0	1	set
1	0	1	0	reset
1	1	invalid		$(Q=\bar{Q}=0)$

S R Q $\bar{Q}$


D
S
R
Q
= D


D
S
R
Q

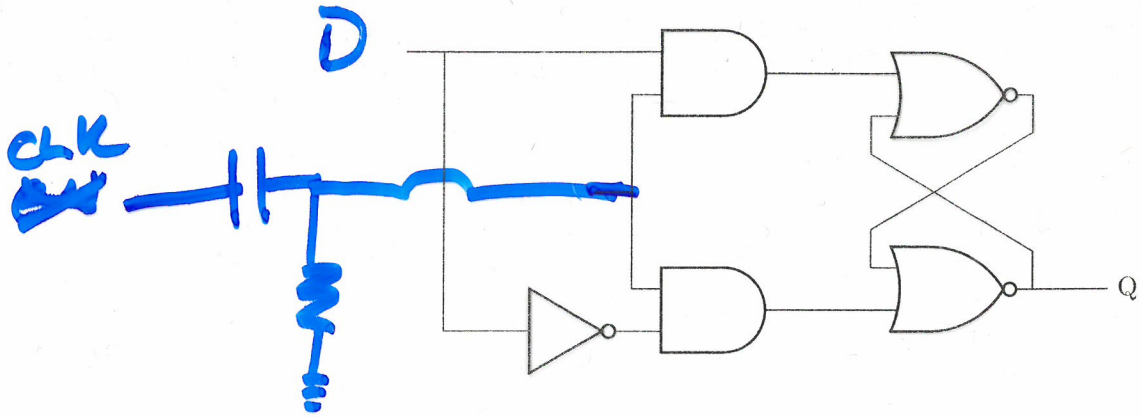


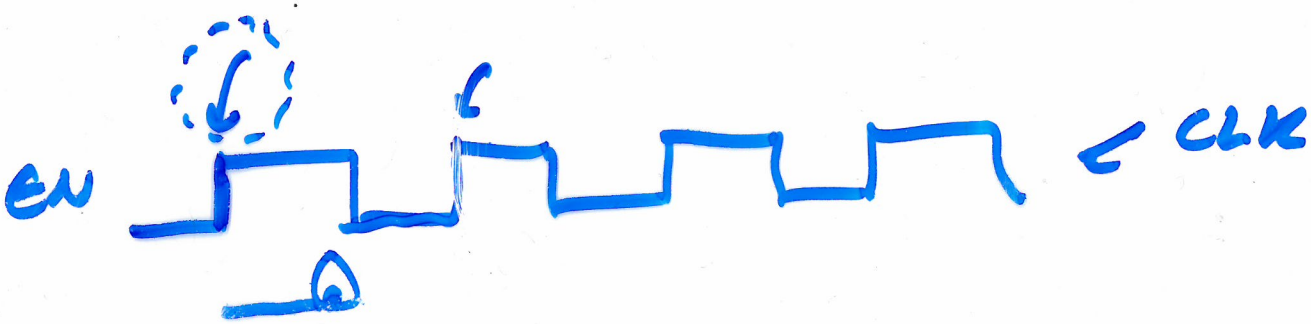
enable

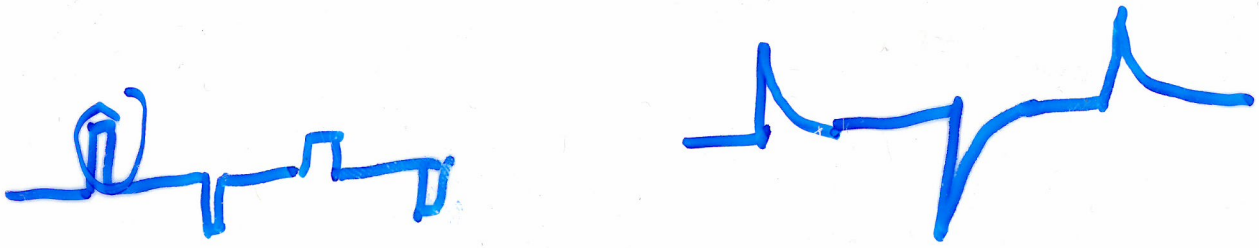
D Latch

D, EN Q

D	EN	Q
0	0	hold
0	1	0
1	0	hold
1	1	1

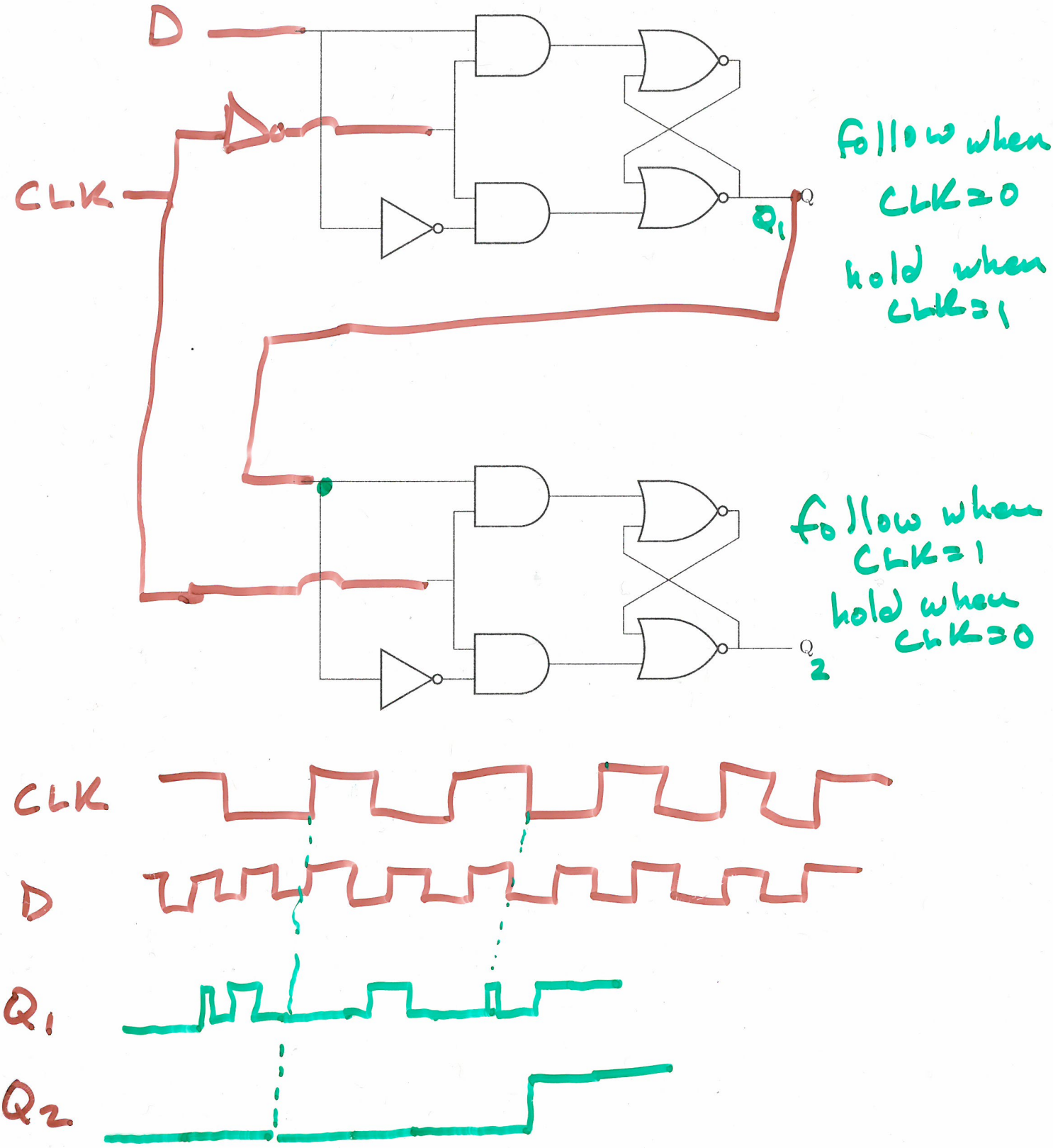


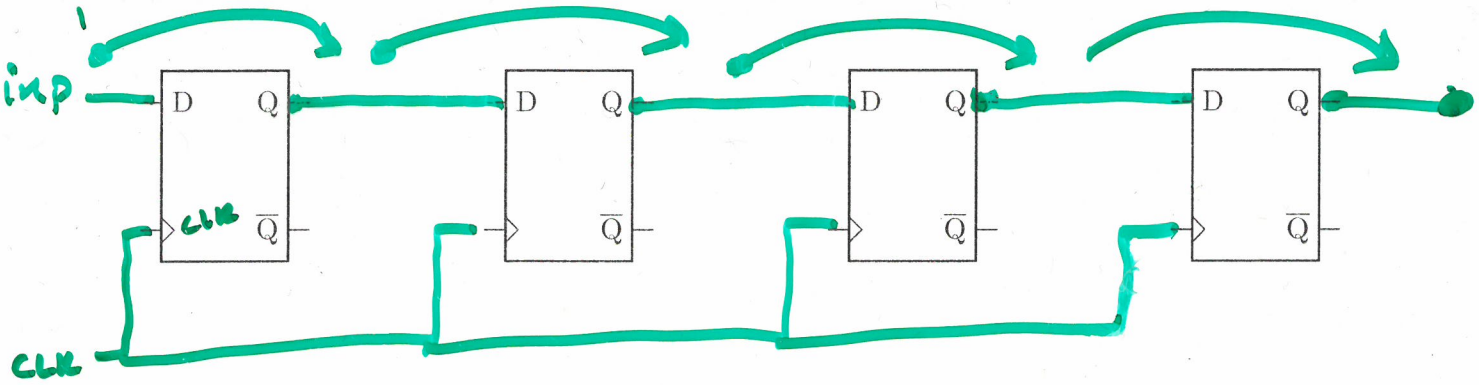




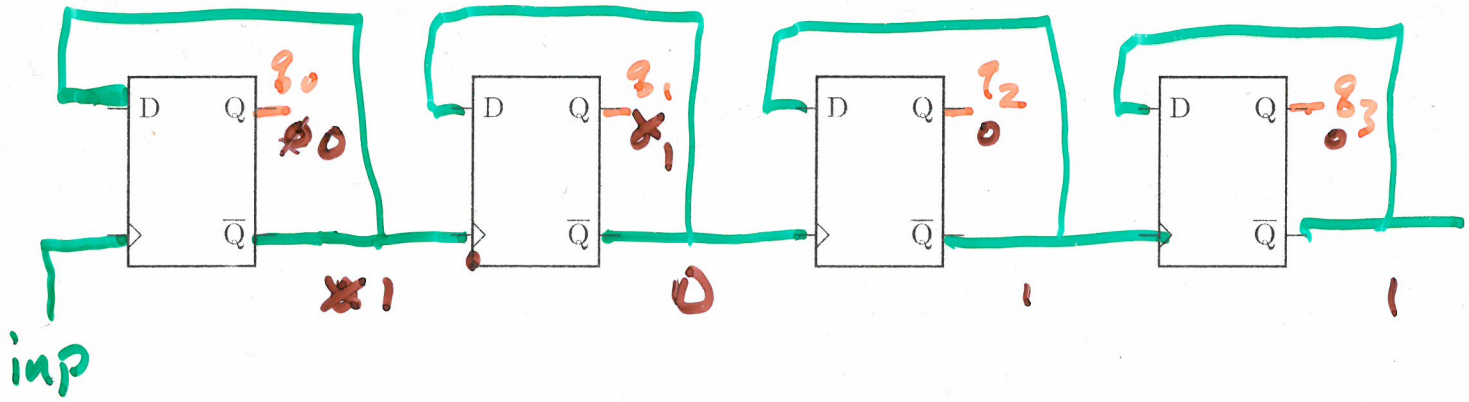
D flip-flop

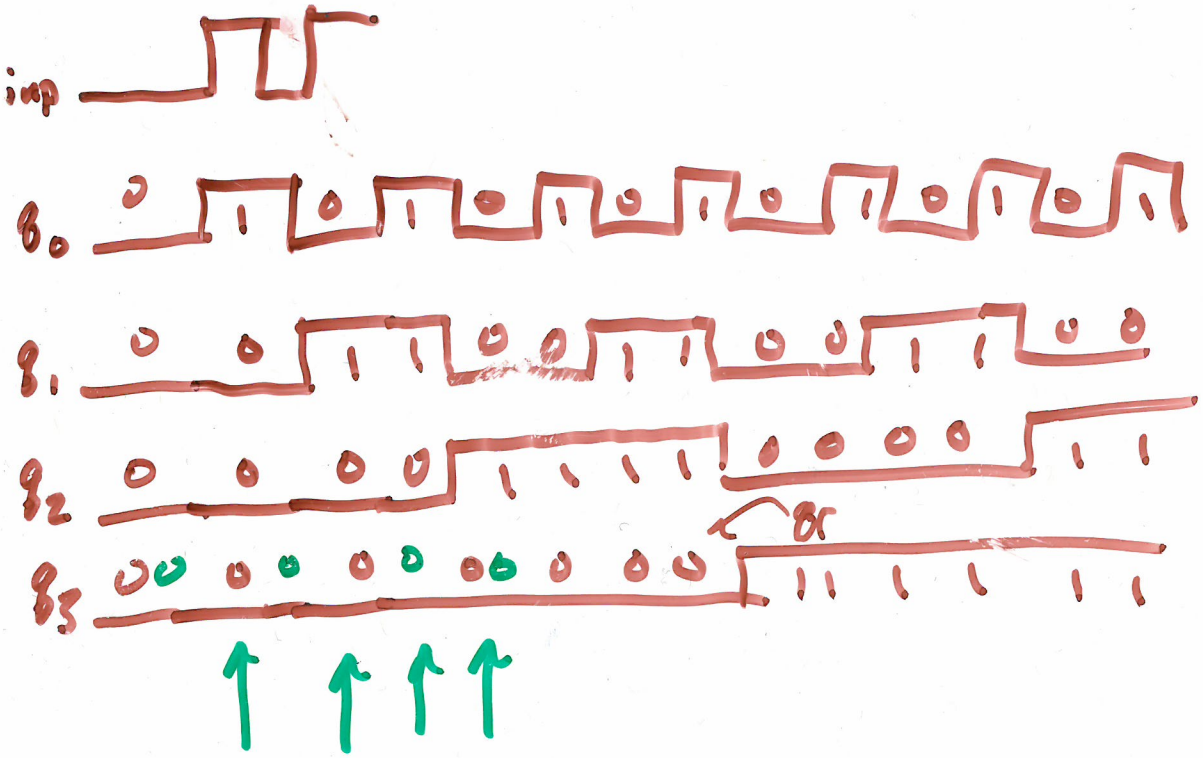
D, CLK Q


D
CLK
Q
Q_1
follow when CLK=0
hold when CLK=1
follow when CLK=1
hold when CLK=0
Q_2
CLK
D
Q_1
Q_2



shift register





inp q_0 q_2