

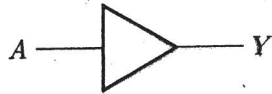
Build a Digital Clock from the 1980's

Lecture 2B: Making Circuits That Remember Stuff



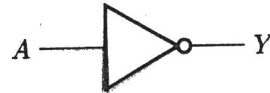
Original photo from <https://alum.mit.edu/slice/tim-beaver-exclusive-interview>
Edited using the GNU Image Manipulation Program (<https://www.gimp.org/>)

YES Gate



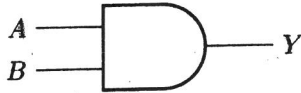
A	Y
0	0
1	1

NOT Gate



A	Y
0	1
1	0

AND Gate



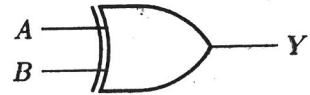
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate



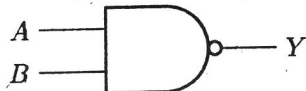
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

XOR Gate



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

NAND Gate



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate

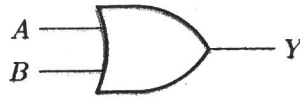


A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

XNOR Gate



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1



SDLS100

**SN5432, SN54LS32, SN54S32,
SN7432, SN74LS32, SN74S32**
QUADRUPL 2-INPUT POSITIVE-OR GATES
DECEMBER 1983 - REVISED MARCH 1988

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	$R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pf}$		14	22	ns
t_{PHL}					14	22	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

